Electronic Design Automation (EDA)

Outline

• Design Flow
  – Hardware description languages (HDL), e.g., verilog and VHDL
• Programmable Logic
  – PALs and PLAs
  – FPGAs
Simplified Design Flow

Design Problem

Design Circuit

Verify/Simulate Functionality (Debugging)

A description (or a model) of a circuit

Schematic

Hardware Description Language (HDL)

Verilog or HDL

```
module circuit (a0,a1,a2,y);
input a0, a1, a2;
output y;
wire w1, w2;
assign w1 = a0&a1;
assign w2 = ~a2;
assign y = w1&w2;
endmodule
```

This can be used to simulate design or to implement in hardware.
Hardware Technologies

• Programmable Logic Devices (PLDs)
  – Programmable Read Only Memory (PROM). Erasable PROMs (EPROMS)
  – Programmable Arrayed Logic (PALs) and Programmable Logic Arrays (PLAs)*
• Field Programmable Gate Arrays (FPGAs)*
• Application Specific ICs (ASICs)

Note that the next set of slides are (heavily) modified versions of slides found at http://subjects.ee.unsw.edu.au/~elec1041 by Saeid Nooshabadi
The originals were adapted from R. Katz’s Contemporary Logic Design
Programmable Logic Arrays (PLAs)

- Programmable technology for combinatorial logic
  \textit{Sum of Products}
- Array of ANDs followed by an array of ORs. Prefabricated
- Programmable by deleting connections at intersections

Programmable Array Logic (PALs)

- Each OR has its own set of ANDs (product terms)
- Easier to build, faster, and most cases it isn’t much of a limitation
PLD (Programmable Logic Devices)

- Registered PAL
- Can implement a Mealy or Moore circuit
- These things can be big:
  - Complex PLDs (CPLDs)

Field-Programmable Gate Arrays

- **Logic blocks**
  - To implement small combinational and sequential circuits
- **Interconnect**
  - Wires and switches to connect logic blocks to each other and to inputs/outputs
- **I/O blocks**
  - Special logic blocks at periphery of device for external connections
Xilinx FPGAs

- CLB - Configurable Logic Block
  - 5-input, 1 output function
  - or 2 4-input, 1 output functions
  - optional register on output

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Can be configured to any small combinational or sequential circuit. In the case of comb circuits, the flip flops are bypassed.

Example configuration

Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)
Xilinx 4000 Interconnect

We can connect CLBs and IOBs by using wires and PSMs.

Figure 28: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)

Xilinx 4000 IOB

Similar to CLB but it's used to connect pins of the chip with the internal circuit.

Pad can be programmed as an input or output.

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Final Comments

• ASICs
  – Usually cheaper (in bulk) and better performance
  – Goes to foundary and takes time. Better once final design is done -- no changes

• FPGAs
  – Better for very rapid design and redesign. Good for prototyping but also end design.
  – Better for small numbers of products
  – More expensive, and less in performance