Objective: You will simulate and build a 3-bit arithmetic logic unit (ALU), shown below, in a field programmable gated array (FPGA). This will give you more experience with designing and implementing circuits with modern tools.

```verilog
module ALU(result, select, a, b);

input [2:0] a, b;
input [2:0] select;
output [2:0] result;

reg [2:0] result;

always @(a or b or select)
begin
  case(select)
    0: result = a&b;
    1: result = a|b;
    2: result = a+b;
    6: result = a-b;
    7: result = (a-b)>>2;
    default: result = 0;
  endcase
end
endmodule
```

Instructions: Follow the procedure below. Demonstrate that you successfully implemented the two steps to the TA. Write a report about the lab assignment and include the verilog modules for the ALU, decoder, and up counter.
**Procedure:** There are two steps.

**Step 1.** Use the XSA board to implement its FPGA as follows. The Decoder decodes the 3 bit value from the ALU into a display on the 7 segment display. In particular, 000, 001,..., 111, from the ALU is displayed as “0”, “1”, ...., “7”, respectively, on the 7 segment display.

**Step 2.** Use the XSA board to implement its FPGA as follows. This is a modification of Step 1 with the addition of a 3-bit up counter.