8 PROGRAMMABLE TIMER, RTI, AND PULSE ACCUMULATOR

This section describes the 16-bit programmable timer, the real time interrupt, and the pulse accumulator system.

8.1 Programmable Timer

The timer has a single 16-bit free-running counter which is clocked by the output of a four-stage prescaler (divide by 1, 4, 8, or 16), which is in turn driven by the MCU clock. Input functions are called input captures. These input captures record the count from the free-running counter in response to a detected edge on an Input line. Output functions, called output compares, cause an output action when there is a match between a 16-bit output-compare register and the free-running counter. This timer system has three input capture registers and five output compare registers.

8.1.1 Counter

The key element in the timer system is a 16-bit free-running counter, or timer counter register. After reset, the MCU is configured to use the E clock as the input to the free-running counter. Initialization software may optionally reconfigure the system to use one of the three prescaler values. The prescaler control bits can only be written once during the first 64 cycles after a reset. Software can read the counter at any time without affecting its value because it is clocked and read during opposite phases of the E clock.

A counter read should first address the most significant byte. An MPU read of this address causes the least significant byte to be transferred to a buffer. This buffer is not affected by reset and is accessed when reading the least significant byte of the counter. For double byte read instructions, the two accesses occur on consecutive bus cycles.

The counter is cleared to $0000 during reset and is a read-only register with one exception. In test modes only, any MPU write to the most significant byte presets the counter to $FFFFF regardless of the value involved in the write.

When the count changes from $FFFF to $0000, the timer overflow flag (TOF) bit is set in timer interrupt flag register 2 (TFLG2). An interrupt can be enabled by setting the interrupt enable bit (TOI) in timer interrupt mask register 2 (TMSK2).

8.1.2 Input Capture

The input capture registers are 16-bit read-only registers which are not affected by reset and are used to latch the value of the counter when a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers counter transfer is defined by the corresponding input edge bits (EDGxB, EDGxA) in TCTL2.
The result obtained by an input capture corresponds to the value of the counter one E clock cycle after the transition which triggered the edge-detection logic. The selected edge transition sets the ICxF bit in timer interrupt flag register 1 (TFLG1) and can cause an interrupt if the corresponding ICx1 bit(s) is (are) set in the timer interrupt mask register 1 (TMSK1). A read of the input capture register's most significant byte inhibits captures for one E cycle to allow a double byte read of the full 16 bit register.

8.1.3 Output Compare

All output compare registers are 16-bit read/write registers which are initialized to $FFFFFF by reset. They can be used as output waveform controls or as elapsed time indicators. If an output compare register is not used, it may be used as a storage location.

All output compare registers have a separate dedicated comparator for comparing against the free-running counter. If a match is found, the corresponding output compare flag (OCxF) bit in TFLG1 is set and a specified action is automatically taken. For output compare functions two through five the automatic action is controlled by pairs of bits (OMx and OLx) in the timer control register 1 (TCTL1). Each pair of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. The output action is taken on each successful compare regardless of whether or not the OCx+ flag was previously clear.

An interrupt can also accompany a successful output compare, provided that the corresponding interrupt enable bit (OCxI) is set in TMSK1.

After a write cycle to the most significant byte, output compares are inhibited for one E cycle in order to allow writing two consecutive bytes before making the next comparison. If both bytes of the register are to be changed, a double-byte write instruction should be used in order to take advantage of the compare inhibit feature.

Writes can be made to either byte of the output compare register without affecting the other byte.

A write-only register, timer compare force (CFORC), allows forced compares. Five of the bit positions in the CFORC register correspond to the five output compares. To force a compare, or compares, a write is done to CFORC register with the associated bits set for each output compare that is to be forced. The action taken as a result of a forced compare is the same as if there was a match between the OCx register and the free-running counter, except that the corresponding interrupt status flag bits are not set. Output actions are synchronized to the prescaled timer clock so there could be as much as 16 E clock cycles of delay between the write to CFORC and the output action.

8.1.4 Output Compare 1 I/O Pin Control

Unlike the other four output compares, output compare 1 can automatically affect any or all of the five output pins (bits 3-7) in port A as a result of a successful compare between the OC1 register and the 16-bit free-running counter. The two 5-bit registers used in conjunction with this function are the output compare 1 mask register (OC1M) and the output compare 1 data register (OC1D).
Register OC1M is used to specify the bits of port A (I/O and timer port) which are to be affected as a result of a successful OC1 compare. Register OC1D is used to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare. If an OC1 compare and another output compare occur during the same E cycle and both attempt to alter the same port A line, the OC1 compare prevails.

This function allows control of multiple I/O pins automatically with a single output compare.

Another intended use for the special I/O pin control on output compare 1 is to allow more than one output compare to control a single I/O pin. This allows pulses as short as one E clock cycle to be generated.

8.1.5 Timer Compare Force Register (CFORC)

The timer compare force register is used to force early output compare actions. The CFORC register is an 8-bit write-only register. Reads of this location have no meaning and always return logic zeros. Note that the compare force function is not generally recommended for use with the output toggle function because a normal compare occurring immediately before or after the force may result in undesirable operation.

<table>
<thead>
<tr>
<th>$100B</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FOC1</td>
<td>FOC2</td>
<td>FOC3</td>
<td>FOC4</td>
<td>FOC5</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

FOC1-FOC5 — Force Output Compare x Action
0 = Has no meaning
1 = Causes action programmed for output compare x, except the OCxF flag bit is not set.

Bits 2-0 — Not Implemented
These bits always read zero.

8.1.6 Output Compare 1 Mask Register (OC1M)

This register is used in conjunction with output compare 1 to specify the bits of port A which are affected as a result of a successful OC1 compare.

<table>
<thead>
<tr>
<th>$100C</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OC1M7</td>
<td>OC1M6</td>
<td>OC1M5</td>
<td>OC1M4</td>
<td>OC1M3</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The bits of the OC1M register correspond bit-for-bit with the lines of port A (lines 7 through 3 only). For each bit that is affected by the successful compare, the corresponding bit in OC1M should be set to one.
Note that the pulse accumulator function shares line 7 of port A. If the DDRA7 bit in the pulse accumulator control register (PACTL) is set, then port A line 7 is configured as an output and OC1 can obtain access by setting OC1M bit 7. In this condition if the PAE bit in the PACTL register is set, enabling the pulse accumulator input, then OC1 compares cause a write of OC1D bit 7 to an internal latch, and the output of that latch drives the pin and the pulse accumulator input. This action can then cause the pulse accumulator to take the appropriate action (pulse count or gate modes).

8.1.7 Output Compare 1 Data Register (OC1D)

This register is used in conjunction with output compare 1 to specify the data which is to be stored to the affected bits of port A as the result of a successful OC1 compare.

<table>
<thead>
<tr>
<th>S1000</th>
<th>OC1U7</th>
<th>OC1U6</th>
<th>OC1U5</th>
<th>OC1U4</th>
<th>OC1U3</th>
<th>OC1U2</th>
<th>OC1U1</th>
<th>OC1U0</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

The bits of the OC1D register correspond bit-for-bit with the lines of port A (lines 7 thru 3 only). When a successful OC1 compare occurs, for each bit that is set in OC1M, the corresponding data bit in OC1D is stored in the corresponding bit of port A. If there is a conflicting situation where an OC1 compare and another output compare function occur during the same E cycle with both attempting to alter the same port A line, the OC1 action prevails.

8.1.8 Timer Control Register 1 (TCTL1)

<table>
<thead>
<tr>
<th>S1020</th>
<th>OM2</th>
<th>OL2</th>
<th>OM3</th>
<th>OL3</th>
<th>OM4</th>
<th>OL4</th>
<th>OM5</th>
<th>OL5</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

OM2, OM3, OM4, and OM5 — Output Mode
OL2, OL3, OL4, and OL5 — Output Level
These two control bits (OMx and OLx) are encoded to specify the output action taken as a result of a successful OCx compare.

<table>
<thead>
<tr>
<th>OMx</th>
<th>OLx</th>
<th>Action Taken Upon Successful Compare</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Timer disconnected from output pin logic</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Toggle OCx output line</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Clear OCx output line to zero</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Set OCx output line to one</td>
</tr>
</tbody>
</table>
8.1.9 Timer Control Register 2 (TCTL2)

<table>
<thead>
<tr>
<th>$1021</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 7-6 — Not Implemented
These bits always read zero.

EDGxB and EDGxA — Input Capture x Edge Control.
These two bits (EDGxB and EDGxA) are cleared to zero by reset and are encoded to configure the input sensing logic for input capture x as follows:

<table>
<thead>
<tr>
<th>EDGxB</th>
<th>EDBxA</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Capture disabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Capture on rising edges only</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Capture on falling edges only</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Capture on any (rising or falling) edge</td>
</tr>
</tbody>
</table>

8.1.10 Timer Interrupt Mask Register 1 (TMSK1)

<table>
<thead>
<tr>
<th>$1022</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

OCxI — Output Compare x Interrupt
If the OCxI enable bit is set when the OCF flag bit is set, a hardware interrupt sequence is requested.

ICxI — Input Capture x Interrupt
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

8.1.11 Timer Interrupt Flag Register 1 (TFLG1)

Timer interrupt flag register 1 is used to indicate the occurrence of timer system events, and together with the TMSK1 register allows the timer subsystem to operate in a polled or interrupt driven system. For each bit in TFLG1, there is a corresponding bit in TMSK1 in the same bit position. If the mask bit is set, each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

These timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read-modify-write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.
OCxF — Output Compare x Flag
This flag bit is set each time the timer counter matches the output compare register x value. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

ICxF — Input Capture x Flag
This flag is set each time a selected active edge is detected on the ICx input line. A write of a zero does not affect this bit. A write of a one causes this bit to be cleared.

8.1.12 Timer Interrupt Mask Register 2 (TMSK2)
Timer interrupt mask register 2 is used to control whether or not a hardware interrupt sequence is requested as a result of a status bit being set in timer interrupt flag register 2. In addition, two timer prescaler bits are included in this register. For each of the four most significant bits in timer flag register 2, (TFLG2), there is a corresponding bit in the timer mask register 2 (TMSK2) in the same bit position.

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF = 1

RTII — RTI Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF = 1

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF = 1

PAII — Pulse Accumulator Input Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF = 1

Bits 3 and 2 — Not Implemented
These bits always read zero.
PR1 and PR0 — Timer Prescaler Selects
These two bits may be read at any time but may only be written during initialization. Writes are disabled after the first write or after 64 E cycles out of reset. If the MCU is in special test or special bootstrap mode, then these two bits may be written any time. These two bits specify the timer prescaler divide factor.

<table>
<thead>
<tr>
<th>PR1</th>
<th>PR0</th>
<th>Prescaler</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>÷ 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>÷ 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>÷ 8</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>÷ 16</td>
</tr>
</tbody>
</table>

8.1.13 Timer Interrupt Flag Register 2 (TFLG2)
Timer interrupt flag register 2 is used to indicate the occurrence of timer system events and, together with the TMSK2 register, allows the timer subsystems to operate in a polled or interrupt driven system. For each bit in timer flag register 2 (TFLG2), there is a corresponding bit in timer mask register 2 (TMSK2) in the same bit position. If the enable bit is set each time the conditions for the corresponding flag are met, a hardware interrupt sequence is requested as well as the flag bit being set.

The timer system status flags are cleared by writing a one to the bit positions corresponding to the flag(s) which are to be cleared. Bit manipulation instructions would be inappropriate for flag clearing because they are read modify write instructions. Even though the instruction mask implies that the programmer is only interested in some of the bits in the manipulated location, the entire location is actually read and rewritten which may clear other bits in the register.

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOF</td>
<td>RTIF</td>
<td>PAOVF</td>
<td>PAIF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TFLG2

RESET 0 0 0 0 0 0 0 0

TOF — Timer Overflow
This bit is cleared by reset. It is set to one each time the 16-bit free-running counter advances from a value of $FFFF$ to $0000$. This bit is cleared by a write to the TFLG2 register with bit 7 set.

RTIF — Real Time Interrupt Flag
This bit is set at each rising edge of the selected tap point. This bit is cleared by a write to the TFLG2 register with bit 6 set.

PAOVF — Pulse Accumulator Overflow Interrupt Flag
This bit is set when the count in the pulse accumulator rolls over from $FF$ to $00$. This bit is cleared by a write to the TFLG2 register with bit 5 set.
PAIF — Pulse Accumulator Input Edge Interrupt Flag
  This bit is set when an active edge is detected on the PAI input pin. This bit is cleared
  by a write to the TFLG2 register with bit 4 set.

Bits 3-0 — Not Implemented
  These bits always read zero.

8.2 Real-Time Interrupt
  The real-time interrupt feature on the MCU is configured and controlled by using two
  bits (RTR1 and RTR0) in the PACTL register to select one of four interrupt rates. The
  RTII bit in the TMSK2 register enables the interrupt capability. Every timeout causes
  the RTIF bit in TFLG2 to be set, and if RTII is set, an interrupt request is generated.
  After reset, one entire real time interrupt period elapses before the RTIF flag is set for
  the first time.

8.3 Pulse Accumulator
  The pulse accumulator is an 8-bit read/write counter which can operate in either of two
  modes (external event counting or gated time accumulation) depending on the state
  of the PAMOD control bit in the PACTL register. In the event counting mode, the 8-bit
  counter is clocked to increasing values by an external pin. The maximum clocking rate
  for the external event counting mode is E clock divided by two. In the gated time ac-
  cumulation mode, a free-running E clock/64 signal drives the 8-bit counter, but only
  while the external PAI input pin is enabled.

  The pulse accumulator uses port A bit 7 as its PAI input, but this pin also shares func-
  tion as a general purpose I/O pin and as a timer output compare pin. Normally port A
  bit 7 would be configured as an input when being used for the pulse accumulator. Note
  that even when port A bit 7 is configured for output, this pin still drives the input to the
  pulse accumulator.

8.3.1 Pulse Accumulator Control Register (PACTL)
  Four bits in this register are used to control an 8-bit pulse accumulator system and two
  other bits are used to select the rate for the real time interrupt system.

<table>
<thead>
<tr>
<th>$1026</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

DDRA7 — Data Direction for Port A Bit 7
  0 = Input only
  1 = Output

PAEN — Pulse Accumulator System Enable
  0 = Pulse accumulator off
  1 = Pulse accumulator on
PAMOD — Pulse Accumulator Mode
  0 = External event counting
  1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control
  This bit has different meanings depending on the state of the PAMOD bit.

<table>
<thead>
<tr>
<th>PAMOD</th>
<th>PEDGE</th>
<th>Action on Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>PAI Falling Edge increments the Counter</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>PAI Rising Edge increments the Counter</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>A zero on PAI inhibits counting</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>A one on PAI inhibits counting</td>
</tr>
</tbody>
</table>

Bits 3-2 — Not Implemented
  These bits always read zero.

RTR1 and RTR0 — RTI Interrupt Rate Selects
  These two bits select one of four rates for the real time periodic interrupt circuit (see Table 8-1). Reset clears these two bits and after reset, a full RTI period elapses before the first RTI interrupt.

Table 8-1 Real Time Interrupt Rate versus RTR1 and RTR0

<table>
<thead>
<tr>
<th>RTR1</th>
<th>RTR0</th>
<th>Rate</th>
<th>XTAL = 12.0 MHz</th>
<th>XTAL = 2^3</th>
<th>XTAL = 8.0 MHz</th>
<th>XTAL = 4.9152 MHz</th>
<th>XTAL = 4.0 MHz</th>
<th>XTAL = 3.6864 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>2^13 + E</td>
<td>8.192 ms</td>
<td>3.91 ms</td>
<td>4.10 ms</td>
<td>6.67 ms</td>
<td>8.19 ms</td>
<td>8.89 ms</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2^14 + E</td>
<td>16.384 ms</td>
<td>7.81 ms</td>
<td>8.19 ms</td>
<td>13.33 ms</td>
<td>16.38 ms</td>
<td>17.78 ms</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2^15 + E</td>
<td>32.768 ms</td>
<td>15.62 ms</td>
<td>16.38 ms</td>
<td>26.67 ms</td>
<td>32.77 ms</td>
<td>35.56 ms</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2^16 + E</td>
<td>65.536 ms</td>
<td>31.25 ms</td>
<td>32.77 ms</td>
<td>53.33 ms</td>
<td>65.54 ms</td>
<td>71.11 ms</td>
</tr>
</tbody>
</table>

E = 3.0 MHz  2.1 MHz  2.0 MHz  1.2288 MHz  1.0 MHz  921.6 kHz