5 SERIAL COMMUNICATIONS INTERFACE

This section contains a description of the serial communication interface (SCI).

5.1 Overview and Features

A full-duplex asynchronous Serial Communications Interface (SCI) is provided with a standard NRZ format (one start bit, eight or nine data bits, and one stop bit) and a variety of baud rates. The SCI transmitter and receiver are functionally independent, but use the same data format and bit rate. “Baud” and “bit rate” are used synonymously in the following description.

5.1.1 SCI Two-Wire System Features

- Standard NRZ (mark/space) format.
- Advanced error detection method includes noise detection for noise duration of up to 1/16 bit time.
- Full-duplex operation.
- Software programmable for one of 32 different baud rates.
- Software selectable word length (eight or nine bit words).
- Separate transmitter and receiver enable bits.
- Capable of being interrupt driven.
- Four separate enable bits available for interrupt control.

5.1.2 SCI Receiver Features

- Receiver wake-up function (idle or address bit).
- Idle line detect.
- Framing error detect.
- Noise detect.
- Overrun detect.
- Receiver data register full flag.

5.1.3 SCI Transmitter Features

- Transmit data register empty flag.
- Transmit complete flag.
- Send break.

5.2 Data Format

Receive data or transmit data is the serial data which is transferred to the internal data bus from the receive data input pin (RxD), or from the internal bus to the transmit data output pin (TxD).

The non-return-to-zero (NRZ) data format shown in Figure 5-1 is used and must meet the following criteria:
1. The idle line is brought to a logic one state prior to transmission/reception of a character.
2. A start bit (logic zero) is used to indicate the start of a frame.
3. The data is transmitted and received least-significant-bit first.
4. A stop bit (logic one) is used to indicate the end of a frame. A frame consists of a start bit, a character of eight or nine data bits, and a stop bit.
5. A break is defined as the transmission or reception of a low (logic zero) for at least one complete frame time.

![Diagram of data format]

* CONTROL BIT M IN SCCR1 SELECTS EITHER 8-BIT OR 9-BIT DATA.

Figure 5-1 Data Format

5.3 Wake-Up Feature

The receiver wake-up feature reduces SCI service overhead in multiple receiver systems. Software in each receiver evaluates the first character(s) of each message. If the message is intended for a different receiver, the SCI can be placed in a sleep mode so that the rest of the message will not generate requests for service. Whenever a new message is started, logic in the sleeping receivers causes them to wake up so they can evaluate the initial character(s) of the new message.

A sleeping SCI receiver can be configured (using the WAKE control bit in serial communications control register 1 (SCCR1)) to wake up using either of two methods: idle line wake up or address mark wake up.

In idle line wake up, a sleeping receiver wakes up as soon as the RxD line becomes idle. Idle is defined as a continuous logic high on the RxD line for ten (or eleven) full bit times. Systems using this type of wake up must provide at least one character time of idle between messages to wake up sleeping receivers but must not allow any idle time between characters within a message.

In address mark wake up, the most significant bit (MSB) in a character is used to indicate that the character is an address (1) or a data (0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wake up would set the MSB of the first character in each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wake up method.

5.4 Receive Data (RxD)

Receive data is the serial data which is applied through the input line and the serial communications interface to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate and this time is referred to as the RT clock.
Once a valid start bit is detected, the start bit, each data bit, and the stop bit are sampled three times at RT intervals 8 RT, 9 RT, and 10 RT (1 RT is the position where the bit is expected to start), as shown in Figure 5-2. The value of the bit is determined by voting logic which takes the value of the majority of samples.

<table>
<thead>
<tr>
<th>PREVIOUS BIT</th>
<th>PRESENT BIT</th>
<th>NEXT BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>RxD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 1</td>
<td>8 9 10</td>
<td>16 1</td>
</tr>
<tr>
<td>R R</td>
<td>R R R</td>
<td>R R</td>
</tr>
<tr>
<td>T T</td>
<td>T T T</td>
<td>T T</td>
</tr>
</tbody>
</table>

Figure 5-2 Sampling Technique Used on All Bits

5.5 Start Bit Detection

When the RxD input is detected low, it is tested for three more sample times (referred to as the start edge verification samples in Figure 5-3). If at least two of these three verification samples detect a logic zero, a valid start bit has been detected, otherwise the line is assumed to be idle. A noise flag is set if all three verification samples do not detect a logic zero. A valid start bit could be assumed with a set noise flag present.

If there has been a framing error without detection of a break (10 zeros for 8-bit format or 11 zeros for 9-bit format), the circuit continues to operate as if there actually was a stop bit and the start edge will be placed artificially. The last bit received in the data shift register is inverted to a logic one, and the three logic one start qualifiers (shown in Figure 5-3) are forced into the sample shift register during the interval when detection of a start bit is anticipated (see Figure 5-4); therefore, the start bit will be accepted no sooner than it is anticipated.

If the receiver detects that a break produced the framing error, the start bit will not be artificially induced and the receiver must actually detect a logic one before the start bit can be recognized. See Figure 5-5.
Figure 5-3  Examples of Start Bit Sampling Techniques

(a) Case 1, Receive Line Low During Artificial Edge

(b) Case 2, Receive Line High During Expected Start Edge

Figure 5-4  SCI Artificial Start Following a Framing Error

Figure 5-5  SCI Start Bit Following a Break
5.6 Transmit Data (TxD)

Transmit data is the serial data from the internal data bus which is applied through the serial communications interface to the output line. The transmitter generates a bit time by using a derivative of the RT clock, thus producing a transmission rate equal to 1/16 that of the receiver sample clock.

5.7 Functional Description

A block diagram of the SCI is shown in Figure 5-6. The user has option bits in serial communications control register 1 (SCCR1) to determine the “wake-up” method (WAKE bit) and data word length (M bit) of the SCI. Serial communications control register 2 (SCCR2) provides control bits which individually enable/disable the transmitter or receiver (TE and RE, respectively), enable system interrupts (TIE, TCIE, ILIE) and provide the wake-up enable bit (RWU) and the send break code bit (SBK). The baud rate register (BAUD) bits allow the user to select different baud rates which may be used as the rate control for the transmitter and receiver.

Data transmission is initiated by a write to the serial communications data register (SCDR). Provided the transmitter is enabled, data stored in the SCDR is transferred to the transmit data shift register. This transfer of data sets the TDRF bit of the SCI status register (SCSR) and may generate an interrupt if the transmit interrupt is enabled. The transfer of data to the transmit data shift register is synchronized with the bit rate clock (Figure 5-7). All data is transmitted LSB first. Upon completion of data transmission, the transmission complete (TC) bit of the SCSR is set (provided no pending data, preamble, or break is to be sent), and an interrupt may be generated if the transmit complete interrupt is enabled. If the transmitter is disabled, and the data, preamble, or break (in the transmit shift register) has been sent, the TC bit will also be set. This will also generate an interrupt if the TCIE bit is set. If the transmitter is disabled in the middle of a transmission, that character will be completed before the transmitter gives up control of the TxD pin.

When the SCDR is read, it contains the last data byte received, provided that the receiver is enabled. The RDRF bit of the SCSR is set to indicate that a data byte has been transferred from the input serial shift register to the SCDR, which can cause an interrupt if the receiver interrupt is enabled. The data transfer from the input serial shift register to the SCDR is synchronized by the receiver bit rate clock. The OR (over-run), NF (noise), or FE (framing) error bits of the SCSR may be set if data reception errors occurred.

An idle line interrupt is generated if the idle line interrupt is enabled and the IDLE bit (which detects idle line transmission) of SCSR is set. This allows a receiver that is not in the wake-up mode to detect the end of a message, the preamble of a new message, or to resynchronize with the transmitter. A valid character must be received before the idle line condition or the IDLE bit will not be set and an idle line interrupt will not be generated.

5.8 SCI Registers

There are five registers used in the serial communications interface and the operation of these registers is discussed in the following paragraphs. Reference should be made to the block diagram shown in Figure 5-6.
5.8.1 Serial Communications Data Register (SCDR)

The serial communications data register performs two functions; i.e., it acts as the receive data register when it is read and as the transmit data register when it is written. Figure 5-6 shows this register as two separate registers, namely: the receive data register and the transmit data register.
Figure 5-6 Serial Communications Interface Block Diagram
5.8.2 Serial Communications Control Register 1 (SCCR1)

The serial communications control register 1 (SCCR1) provides the control bits which:
(1) determine the word length, and (2) select the method used for the wake-up feature.

<table>
<thead>
<tr>
<th>$102C</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R8</td>
<td>T8</td>
<td>0</td>
<td>M</td>
<td>WAKE</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RESET</td>
<td>U</td>
<td>U</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

R8 — Receive Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the receive data character.

T8 — Transmit Data Bit 8
If the M bit is set, this bit provides a storage location for the ninth bit in the transmit data character. It is not necessary to write to this bit for every character transmitted, only when the sense is to be different than that for the previous character.

Bit 5 — Not Implemented
This bit always reads zero.

M — SCI Character Length
0 = 1 start bit, 8 data bits, 1 stop bit
1 = 1 start bit, 9 data bits, 1 stop bit

WAKE — Wake Up Method Select
0 = Idle Line
1 = Address Mark

Bits 2-0 — Not Implemented
These bits always read zero.

5.8.3 Serial Communications Control Register 2 (SCCR2)

The serial communications control register 2 (SCCR2) provides the control bits which enable/disable individual SCI functions.

<table>
<thead>
<tr>
<th>$102D</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TIE</td>
<td>TCIE</td>
<td>RIE</td>
<td>ILIE</td>
<td>TE</td>
<td>RE</td>
<td>RWU</td>
<td>SBK</td>
</tr>
<tr>
<td>RESET</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

ILIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt if TDRE = 1
TCIE — Transmit Complete Interrupt Enable
   0 = TC interrupts disabled
   1 = SCI Interrupt if TC = 1

RIE — Receive Interrupt Enable
   0 = RDRF and OR interrupts disabled
   1 = SCI interrupt if RDRF or OR = 1

ILIE — Idle Line Interrupt Enable
   0 = IDLE interrupts disabled
   1 = SCI interrupt if IDLE = 1

TE — Transmit Enable
   When the transmit enable bit is set, the transmit shift register output is applied to the TxD line. Depending on the state of control bit M (SCCR1), a preamble of 10 (M = 0) or 11 (M = 1) consecutive ones is transmitted when software sets the TE bit from a cleared state. After loading the last byte in the serial communications data register and receiving the TDRE flag, the user can clear TE. Transmission of the last byte will then be completed before the transmitter gives up control of the TxD pin. While the transmitter is active, the data direction register control for port D bit 1 is overridden and the line is forced to be an output.

RE — Receive Enable
   When the receive enable bit is set, the receiver is enabled. When RE is clear, the receiver is disabled and all of the status bits associated with the receiver (RDRF, IDLE, OR, NF, and FE) are inhibited. While the receiver is enabled, the data direction register control for port D bit 0 is overridden and the line is forced to be an input.

RWU — Receiver Wake Up
   When the receiver wake-up bit is set by the user’s software, it puts the receiver to sleep and enables the “wake up” function. If the WAKE bit is cleared, RWU is cleared by the SCI logic after receiving 10 (M = 0) or 11 (M = 1) consecutive ones. If the WAKE bit is set, RWU is cleared by the SCI logic after receiving a data word whose MSB is set.

SBK — Send Break
   If the send break bit is toggled set and cleared, the transmitter sends 10 (M = 0) or 11 (M = 1) zeros and then reverts to idle or sending data. If SBK remains set, the transmitter will continually send whole blocks of zeros (sets of 10 or 11) until cleared. At the completion of the break code, the transmitter sends at least one high bit to guarantee recognition of a valid start bit. If the transmitter is currently empty and idle, setting and clearing SBK is likely to produce two character times of break because the first break transfers almost immediately to the shift register and the second is then queued into the parallel transmit buffer.
5.8.4 Serial Communications Status Register (SCSR)

The serial communications status register (SCSR) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt.

<table>
<thead>
<tr>
<th>$102E</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>SCSR</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TDRE</td>
<td>TC</td>
<td>RDRF</td>
<td>IDLE</td>
<td>OR</td>
<td>NF</td>
<td>FE</td>
<td>0</td>
<td>SCSR</td>
</tr>
<tr>
<td>RESET</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

TDRE — Transmit Data Register Empty

The transmit data register empty bit is set to indicate that the content of the serial communications data register has been transferred to the transmit serial shift register. This bit is cleared by reading the SCSR (with TDRE = 1) followed by a write to the SCDR.

TC — Transmit Complete

The transmit complete bit is set at the end of a data frame, preamble, or break condition if:

1. TE = 1, TDRE = 1, and no pending data, preamble, or break is to be transmitted; or
2. TE = 0, and the data, preamble, or break in the transmit shift register has been transmitted.

The TC bit is a status flag which indicates that one of the above conditions have occurred.

The TC bit is cleared by reading the SCSR (with TC set) followed by a write to the SCDR.

RDRF — Receive Data Register Full

The receive data register full bit is set when the receiver serial shift register is transferred to the SCDR. The RDRF bit is cleared when the SCSR is read (with RDRF set) followed by a read of the SCDR.

IDLE — Idle Line Detect

The idle line detect bit, when set, indicates the receiver has detected an idle line. The IDLE bit is cleared by reading the SCSR with IDLE set followed by reading SCDR. Once the IDLE status flag is cleared, it will not be set again until after the RxD line has been active and becomes idle again.

OR — Overrun Error

The overrun error bit is set when the next byte is ready to be transferred from the receive shift register to the SCDR which is already full (RDRF bit is set). When an overrun error occurs, the data which caused the overrun is lost and the data which was already in SCDR is not disturbed. The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCDR.
NF — Noise Flag  
The noise flag bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with NF set), followed by a read of the SCDR.

FE — Framing Error  
The framing error bit is set when no stop bit was detected in the received data character. The FE bit is set at the same time as the RDRF is set. If the byte received causes both framing and overrun errors, the processor will only recognize the overrun error. The framing error flag inhibits further transfer of data into the SCDR until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to one) followed by a read of the SCDR.

Bit 0 — Not Implemented  
This bit always reads zero.

5.8.5 Baud Rate Register (BAUD)  
The baud rate register selects the different baud rates which may be used as the rate control for the transmitter and receiver. The SCP[0:1] bits function as a prescaler for the SCR[0:2] bits. Together, these five bits provide multiple baud rate combinations for a given crystal frequency.

<table>
<thead>
<tr>
<th>$102B</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCLR</td>
<td>0</td>
<td>SCP1</td>
<td>SCP0</td>
<td>RCKB</td>
<td>SCR2</td>
<td>SCR1</td>
<td>SCR0</td>
<td>BAUD</td>
</tr>
<tr>
<td>RESEI</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>U</td>
<td>U</td>
<td>U</td>
<td>U</td>
</tr>
</tbody>
</table>

TCLR — Clear Baud Rate Counters (Test)  
This bit is used to clear the baud rate counter chain during factory testing. TCLR is zero and cannot be set while in normal operating modes.

SCP1 and SCP0 — SCI Baud Rate Prescaler Selects  
The E clock is divided by the factors shown in Table 5-1. This prescaled output provides an input to a divider which is controlled by the SCR2-SCR0 bits.

<table>
<thead>
<tr>
<th>SCP1</th>
<th>SCP0</th>
<th>Internal Processor Clock Divided By</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>13</td>
</tr>
</tbody>
</table>

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects  
These three bits select the baud rates for both the transmitter and the receiver. The prescaler output described above is further divided by the factors shown in Table 5-2.
Table 5-2 Second Prescaler Stage

<table>
<thead>
<tr>
<th>SCR2</th>
<th>SCR1</th>
<th>SCR0</th>
<th>Prescaler Output Divide By</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>64</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>128</td>
</tr>
</tbody>
</table>

RCKB — SCI Baud Rate Clock Check (Test)

This bit is used during factory testing to enable the exclusive-OR of the receiver clock and transmitter clock to be driven out the TxD pin. RCKB is zero and cannot be set while in normal operating modes.

The diagram shown in Figure 5-7 and the data given in Table 5-3 and Table 5-4 illustrate the divider chain used to obtain the baud rate clock. Note that there is a fixed rate divide-by-16 between the receive clock (RT) and the transmit clock (Tx). The actual divider chain is controlled by the combined SCP[1:0] and SCR[2:0] bits in the baud rate register as illustrated.

Figure 5-7 Rate Generator Division

Table 5-3 Prescaler Highest Baud Rate Frequency Output

<table>
<thead>
<tr>
<th>SCP Bit</th>
<th>Clock* Divided By</th>
<th>Crystal Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>12.0</td>
</tr>
<tr>
<td>0 0</td>
<td>1</td>
<td>187.50 K Baud</td>
</tr>
<tr>
<td>0 1</td>
<td>3</td>
<td>62.50 K Baud</td>
</tr>
<tr>
<td>1 0</td>
<td>4</td>
<td>46.875 K Baud</td>
</tr>
<tr>
<td>1 1</td>
<td>13</td>
<td>14.423 K Baud</td>
</tr>
</tbody>
</table>

*The clock in the “Clock Divided By” column is the internal processor clock.
NOTE

The divided frequencies shown in Table 5-3 represent baud rates which are the highest transmit baud rate (Tx) that can be obtained by a specific crystal frequency and only using the prescaler division. Lower baud rates may be obtained by providing a further division using the SCI rate select bits as shown below for some representative prescaler outputs.

<table>
<thead>
<tr>
<th>SCR Bit</th>
<th>Divided</th>
<th>Representative Highest Prescaler Baud Rate Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 1 0</td>
<td>Ry</td>
<td>131.072 K Baud 32.768 K Baud 76.80 K Baud 19.20 K Baud 9600 Baud 4800 Baud</td>
</tr>
<tr>
<td>0 0 1</td>
<td>2</td>
<td>65.538 K Baud 16.384 K Baud 38.40 K Baud 9600 Baud 4800 Baud 2400 Baud</td>
</tr>
<tr>
<td>0 1 0</td>
<td>4</td>
<td>32.768 K Baud 8.192 K Baud 19.20 K Baud 4800 Baud 2400 Baud 1200 Baud</td>
</tr>
<tr>
<td>0 1 1</td>
<td>8</td>
<td>16.384 K Baud 4.096 K Baud 9600 Baud 2400 Baud 1200 Baud 600 Baud</td>
</tr>
<tr>
<td>1 0 0</td>
<td>16</td>
<td>8.192 K Baud 2.048 K Baud 4800 Baud 1200 Baud 600 Baud 300 Baud</td>
</tr>
<tr>
<td>1 0 1</td>
<td>32</td>
<td>4.096 K Baud 1.024 K Baud 2400 Baud 600 Baud 300 Baud 150 Baud</td>
</tr>
<tr>
<td>1 1 0</td>
<td>64</td>
<td>2.048 K Baud 512 Baud 1200 Baud 300 Baud 150 Baud 75 Baud</td>
</tr>
<tr>
<td>1 1 1</td>
<td>128</td>
<td>1.024 K Baud 256 Baud 600 Baud 150 Baud 75 Baud —</td>
</tr>
</tbody>
</table>

NOTE

Table 5-4 illustrates how the SCI select bits can be used to provide lower transmitter baud rates by further dividing the prescaler output frequency. The five examples are only representative samples. In all cases, the baud rates shown are transmit baud rates (transmit clock) and the receiver clock is 16 times higher in frequency than the actual baud rate.