EE 366 CMOS VLSI Design

**Designation:** Elective

**Catalog Description:** EE 366 CMOS VLSI Design (4) (3 Lec, 1 3-hr Lab) Introduction to the design of very large scale integrated (VLSI) systems and use of CAD tools and design languages. Lab includes hands-on use of CAD tools. Pre: 260.

**Credits:** 4 – (2 design credits).

**Pre-requisites:** Digital design basics (EE 260), basic circuit theory (EE211).

**Class/Lab Schedule:** Three 1-hour lectures and one 3-hour lab per week.

**Topics Covered:**

29. **CMOS Basics (20 hr)**
- Introduction to modern digital design and Technology Trends (1 hr).
- Basics of Solid State Physics and MOS Transistors (1½ hr).
- Manufacturing Process and Design Rules (1½ hr).
- CMOS Logic and elementary design (2 hr).
- Types of ASICs and Structured Design (1 hr).
- MOS transistor theory (3 hr).
- CMOS inverter: DC analysis (1½ hr).
- CMOS inverter: transient analysis (1 hr).
- MOS SPICE Models and Simulations (½ hr).
- Delay estimation (RC and Elmore Delay model) (1 hr).
- Delay estimation and Gate sizing (Logical Effort) (2 hr).
- Power Dissipation and Low Power Design (1 hr).
- Interconnect modeling and wire engineering (2 hr).
- Design margin, process variation and Device Scaling (1 hr).

30. **CMOS VLSI Design (14½ hr)**
- CMOS combinational logic – Static, Ratioed, Dynamic, Pass-Transistors Families (2 hr).
- Sequencing Methods (Static, Two-Phase, Time Borrowing, Clock Skew) (1 hr).
- Sequential logic design (2 hr).
- Adders: Single-bit circuits (1 hr).
- Adders: Ripple, Generation and Propagation, Manchester, Carry Skip (1 hr).
- Adders: Look-ahead, Select, Conditional-Sum, Tree (1½ hr).
- Other Arithmetic Building Blocks: One-Zero, Comparators, Counters, Shifters (1 hr).
- Designing Arithmetic Building Blocks: Multipliers (1 hr).
- Array subsystems: SRAM (1 hr).
- Array subsystems: DRAM, ROM, CAM, PLA (1 hr).
- Power Distribution (IR Drop, di/dt noise) and I/O circuits (1 hr).
- Clock generation and Distribution (1 hr).

31. **Hardware Description Languages (10 hr) (chapters from “VHDL – Programming by Example,” book)**
- Hardware description languages: Introduction and Rationale (½ hr).
- VHDL: Hands-on (½ hr).
- VHDL: Basic Terminology and Design Units (1 hr).
- VHDL: Behavioral Modelling (1 hr).
- VHDL: Process Semantics and Interaction (2 hr).
- VHDL: Basic Syntax and Data Types (2 hr).
- VHDL: Subprogram and Packages – the std_logic types (1 hr).
- VHDL: Configurations (1 hr).
- VHDL and synthesis (1 hr).
Textbooks and Other Material:


Course Objectives and Their Relationship to Program Objectives:
The student learns design skills and uses tools that are essential for the practice and theory of design for advanced digital systems. [Program Objectives this course addresses: 1, 2, 3, and 5.]

Course Outcomes
The following are the course outcomes and the subset of Program Outcomes (numbered 1-11 in square braces "[ ]") they address:

- Understand CMOS technology. [1]
- Be able to do DC and transient analysis, of digital CMOS circuits. [1,5]
- Be able to use a circuit simulator (HSPICE) to perform analysis and optimizations of digital circuits. [3,5,11]
- Become proficient in a hardware description language (e.g., VHDL). [3,5,11]
- Be able to do design trade-offs considering area, speed, power and reliability. [5]
- Be able to estimate area and power dissipation. [5]
- Be able to design small ASICs. [3]
- Understand logic synthesizers and be able to synthesize a simple circuit. [11]

Computer Usage:
All the lab assignments are simulations or designs that require operating a computer skillfully. The CAD tools used are installed on a UNIX system.

Design Credits and Features:
There are two design credits. There is a lab component that is dedicated to CMOS VLSI and ASIC design and counts for one of the design credits. About a third of the lectures cover design techniques, methodologies, and tools. Therefore, the lecture component has a design credit.

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Person(s) Preparing Syllabus and Date:  Luca Macchiarulo, November 24, 2008.