EE 461 Computer Organization and Architecture

Credits: 3

Categorization of credits: engineering topic

Instructor: Yingfei Dong. Revised Jan. 8, 2021.

Text Book and Other Required Materials:

"*Computer Organization and Design: The Hardware/Software Interface*" by Patterson and Hennessey. Supplemental readings on latest technology advances and industry news.

Designation: Elective

Catalog Description: EE 461 Computer Organization and Architecture(3) This course introduces the principles of computer organization and the basic architecture concepts. The course emphasizes performance and cost analysis, instruction set design, pipelining, memory technology, memory hierarchy, virtual memory management, and I/O systems. Basic technical writing skills are also taught in this class.

Pre-and Co-requisites: EE 361 "Digital Systems and Computer Design" or consent.

Contact Hours: one hour after the class or email to yingfei@hawaii.edu for appointments

Class/Lab Schedule: 3 lecture hours per week

Topics Covered:

- Computer performance measurement methods, criteria and pitfalls (5 hours)
- Principles of instruction set design, the role of compiler and optimizations, historical perspective on instruction set design (5 hours)
- Principle of pipeline processor, hazards and design considerations (4 hours)
- Exception handling and long latency operations in pipeline design(3 hours)
- Role of compiler and speculative execution on performance (2 hours)
- Instruction level parallelism and processor design (2 hours)
- Memory technology (3 hours)
- Cache design and its impact on performance (4 hours)
- Memory hierarchy, virtual memory and their cost/performance (6 hours)
- I/O systems (5 hours)
- Interconnection networks and fault tolerance (4 hours)
- Technical Writing Basics (6 hours)

Course Objectives and Their Relationship to Program Objectives:

A student should grasp the basic concepts of computer architecture and organization, and understand the key skills of constructing cost-effective computer systems. A student should learn how to quantitatively evaluate different designs and organizations, and provide quantitative arguments in evaluating different designs. A student should be able to articulate design issues in the development of basic computer components that satisfy design requirements and objectives. In addition, a student should experience use of design tools to model various alternatives in computer design. A student should understand the basics of technical writing, and is able to

construct a detailed tutorial paper on a selected topic related to computer engineering. [Program Objectives addressed by this course: 1, 2, and 4.]

Course Outcomes and Their Relationship to Program Outcomes:

The following are the course outcomes and the subset of Program Outcomes (numbered 1-11 in square braces "[ ]") they address:

- Understand the merits and pitfalls in computer performance measurements. [1,6]
- Understand the impact of instruction set architecture on cost-performance of computer design. [1,2,6]
- Design a pipeline for consistent execution of instructions with minimum hazards. [1,2]
- Understand ways to incorporate long latency operations in pipeline design. [1,2]
- Understand ways to take advantage of instruction level parallelism for high performance processor design. [1,2,6]
- Understand dynamic scheduling methods and their adaptation to contemporary microprocessor design. [1,2]
- Understand the impact of branch scheduling techniques and their impact on processor performance. [1,2,7]
- Understand alternatives in cache design and their impacts on cost/performance [1,2]
- Understand contemporary microprocessor designs and identify various design techniques employed. [1,2]
- Design an interconnection networks and multiprocessors. [1,2]
- Understand the design process of a computer and critical elements in each step. [1,2,6]
- Understand memory hierarchy and its impact on computer cost/performance. [1,2]
- Use tools for modeling various microprocessor design alternatives. [1,2,6]
- Discuss current events in the microprocessor R&D and industry [1,2,5,6]
- Verbally demonstrate and communicate findings on processor simulation. [1,3,5,7]

Contribution of Course to Meeting the Professional Component

Engineering Topics: 60% Technical Writing: 40%

Computer Usage: Students use SPIM to simulate the impact on processor performance by changing various design parameters. The Simple Scalar Simulator is a set of simulators that include multi-level cache with different configurations, branch prediction, and out-of-order execution, and generates myriad of meaningful statistics. Students learn to interpret the statistics as well to improve their subsequent designs. The course also makes use of Internet access such as email and the web, for references. The course has a web site, which has downloadable software and documents, as well as reference links. Approximately 20% of the assignments use computers. Much of the assigned problems involve pen and paper analysis of computer performance. Note that some are supplemental reading assignments on the latest developments in computer architecture that are not covered in the textbooks.

Design Credits and Features: EE 461 has 1 design credit. About 50% of the homework assignments are performance-related analysis of computer design choices. About another 10% are in-class discussions of design choices and justifications. The course project involves simulation and analysis of various parameters in computer organization. Another 40% are on technical writing communications skills.